

KWM-001

PATENT APPLICATION

A2  
12. (Amended) The semiconductor device according to claim 10, further comprising:  
a second insulating layer provided between said wiring and a passivation film on the surface of said semiconductor chip to flatten the surface of said wiring.

13. (Amended) The semiconductor device according to claim 10, wherein said wiring is made of an Au, which is provided so as to connect to said electrode terminal via a barrier metal layer, and

wherein said low-melting point metal layer is made of an Au-Sn alloy.

14. (Amended) The semiconductor device according to claim 10, wherein said wiring comprising:

a Cu wiring made of Cu formed simultaneously with said electrode terminal;

a barrier metal layer provided on said Cu wiring; and

an Au wiring provided on said barrier metal layer,

wherein said low-melting point metal layer is made of an Au-Sn alloy and is provided on said Au wire.

15. (Amended) The semiconductor device according to claim 10, wherein said wiring is made of Au formed simultaneously with said electrode terminal, and said low-melting point metal layer is made of an Au-Sn alloy.

16. (Amended) The semiconductor device according to claim 8 or 9, wherein said Au-Sn alloy constituting said joining portion has an Au-rich composition containing at least 65 weight-percent of Au.

17. (Amended) The semiconductor device according to claim claim 8 or 9, wherein an Au-Sn alloy layer of said joining portion has a thickness of  $0.8 \mu\text{m}$  or more and  $5 \mu\text{m}$  or less.

18. (Amended) The semiconductor device according to claim 1 or 2, further comprising:

Sub B5  
an insulating resin layer provided at a gap between said first and second semiconductor chips joined each other to fill the gap, said insulating resin layer having nearly the same elastic modulus as said bump electrode.

19. (Amended) The semiconductor device according to claim 1 or 2, further comprising:

KWM-001

PATENT APPLICATION

A2  
an insulating resin layer having a thermal shrinkage factor of 5% or less, which is provided at a gap between said first and second semiconductor chips joined each other to fill the gap.

20. (Amended) The semiconductor device according to claim 1, wherein a circuit element is formed in a semiconductor layer at said joining portion of at least one of said first and second semiconductor chips.

A3  
24. (Amended) The method according to claim 21 or 22, further comprising the steps of:

alloying said metals provided on the surface of said electrode terminal or said wiring of one of said first and second semiconductor chips with said low-melting point metal layer provided on the surface thereof; and  
joining to the other of said first and second semiconductor chips or substrate.

#### IN THE ABSTRACT:

Please amend Abstract as follows:

A4  
--In a COC type semiconductor device, a bump electrode of a second semiconductor chip is joined to a first semiconductor chip having a bump electrode formed thereon. The bump electrodes and of the respective first and second semiconductor chips and are both made of first metal such as Au having a relatively high melting point, while a joining portion of these bump electrodes and is formed of an alloy layer of the first metal and second metal, which second metal is made of such a material that can melt at a lower temperature than the melting point of the first metal to be alloyed with it. As a result, in the COC type semiconductor device, when interconnecting a plurality of semiconductor chips, their electrode terminals can be joined to each other without deteriorating the properties of these chips owing to the high temperature applied thereon.--